IN THE SPECIFICATION:

Please amend the specification as follows:

Page 2, paragraph 2, please replace with the following:

Another problem lies in the temperature of the heat treatment. Normally, substrates used for fabricating a TFT are roughly divided into those composed of pure silicon oxide such as silica glass and non-alkaline boro-silicated glass such as ~~Coning~~ Corning No. 7059 (hereinafter referred to as ~~Coning~~ Corning 7059). Among them, the former has no problem in terms of temperature because it has an excellent heat resistance and can be handled in the same manner with the wafer process of normal semiconductor integrated circuits. However its cost is high and increases exponentially as the substrate area increases. Accordingly, it is used only for TFT integrated circuits having a relatively small area.

Page 16, paragraph 4, please replace with the following:

The temperature of the thermal crystallization is an important parameter and the crystallinity of a TFT is determined by the temperature in the present invention. Generally, the temperature of thermal annealing is restricted by a substrate and other materials. As far as the restriction of a substrate material is concerned, a thermal annealing of up to 1100°C is possible when silicon and silica are used as a substrate. However, it is desirable to anneal at less than 650°C of temperature in a case of ~~Coning~~ Corning 7059 glass which is a typical non-alkaline glass. However, it must be set considering characteristics required for each TFT, other than the substrate, in the present invention from the aforementioned reasons. When the annealing temperature is high, generally a growth of crystal of TFT advances, the mobility is increased and the leak current increases. Accordingly, the annealing temperature should be 450 to 1000°C or preferably 500 to 800°C in order to obtain TFTs having different characteristics on the same substrate like the present invention.

Page 20, last paragraph, please replace with the following:

A method for fabricating a TFT using a crystal silicon film obtained by crystallizing an amorphous silicon film using a plurality of island nickel films formed on ~~Coning~~ Corning 7059 glass substrate as starting points will be described in the present embodiment. There are two methods for forming the island nickel films depending on whether it is formed on or

under the amorphous silicon film. Fig. 2(A-1) shows the method wherein it is formed under the film and Fig. 2(A-2) shows the method wherein it is formed on the film. What must be careful especially about the later is that because nickel is selectively etched after forming it on the whole surface of the amorphous silicon film in the process, nickel and amorphous silicon react each other and produce nickel silicide, though it is a small amount. Because a good crystalline silicon film which the present invention aims for cannot be obtained if this nickel silicide remains as it is, it is necessary to remove this nickel silicide fully by hydrochloric acid or hydrofluoric acid. Due to that, the amorphous silicon is thinned down from the initial state.

Page 21, paragraph 3, please replace with the following:

In either of the cases, a ground silicon oxide film 1B with a thickness of 2000 angstrom was formed on a substrate 1A (~~Coning~~ Corning 7059) by a plasma CVD method. The amorphous silicon film 1 was fabricated by a plasma CVD method or vacuum CVD method with a thickness of 200 to 3000 angstrom or preferably 500 to 1500 angstrom. The amorphous silicon film was readily crystallized after removing hydrogen by annealing 0.1 to 2 hours at 350 to 450°C to keep the hydrogen concentration within the film to less than 5 atomic percent.

Page 28, last paragraph, please replace with the following:

A ground silicon oxide film 702 (thickness: 2000 angstrom) was formed on a substrate (~~Coning~~ Corning No. 7059) 701 by a sputtering method. Then a silicon film 703 with a thickness of 300 to 800 angstrom or 500 angstrom thick for example was formed. Further, a silicon oxide film 704 was formed by a plasma CVD method. This silicon oxide film 704 acts as a masking material and its thickness was preferred to be 500 to 2000 angstrom. If it is too thin, the crystallization advances from an unexpected location by pinholes and if it is too thick, it takes a time to form the film and is not suited for mass-production. Then it was set at 1000 angstrom here.

Page 33, paragraph 4, please replace with the following:

This process can be implemented by laser annealing. Because a thermal damage on the substrate is small when annealed by laser, a normal non-alkaline glass such as ~~Coning~~ Corning 7059 can be used. Further, at that time, a material having an inferior heat resistance

such as aluminum can be used as a material for the gate electrode. The P-type region 127A and N-type regions 127B and 127C were created by the process described above. A sheet resistance of those regions was 200 to 800 ohm/sheet.

Page 34, paragraph 2, please replace with the following:

Fig. 10 shows the present embodiment. In the present embodiment, a difference of mobility of NMOS and PMOS is reduced in a CMOS circuit utilizing the present invention. At first, a ground oxide film 132 was deposited into a thickness of 20 to 200 nm by a sputtering method on a ~~Coning~~ Corning 7059 substrate 131. Further on that, an amorphous silicon film was deposited into a thickness of 50 to 250 nm by a plasma CVD method or vacuum CVD method using mono-silane or di-silane as an original material. Here, a concentration of oxygen or nitrogen in the amorphous silicon film should have been less than 10^{18} cm^{-2} or preferably less than 10^{17} cm^{-2}. The vacuum CVD method was suited for this purpose. The oxygen concentration was set to be less than 10^{17} cm^{-2} in the present embodiment.

Page 36, last paragraph, please replace with the following:

Fig. 11 shows the present embodiment. The present embodiment relates to a circuit in which a transistor and silicon resistance are combined. Silicon doped by impurity can be used as a protecting circuit of the transistor. At first, a ground oxide film 141 was deposited into a thickness of 20 to 200 nm by a sputtering method on a ~~Coning~~ Corning 7059 substrate 140. Further on that, an amorphous silicon film 142 was deposited into a thickness of 100 to 250 nm by a plasma CVD method or vacuum CVD method using mono-silane or di-silane as an original material. Here, a concentration of oxygen or nitrogen in the amorphous silicon film should have been less than 10^{18} cm^{-2} or preferably less than 10^{17} cm^{-2}.